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PTO/SB/122 (04-05)
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Application Number	10,728,036
Filing Date	December 3, 2003
First Named Inventor	Cam L Lu et al.
Art Unit	2825
Examiner Name	Siek, Vuthe
Attorney Docket Number	03-1978 / 81641

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PTC/SB/96 (08-03)

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STA	ATEMENT UNDER 37 CFR 3.73(b)
Applicant/Patent Owner; LSI Logic Corporation	
Application No./Patent No.: 10,728,036	Filed/Issue Date: December 3, 2003
	ault and Transition Delay Fault Truncated Scan Test Pattern for an Integrated Circuit Design
LSI LOGIC CORPORATION	, a CORPORATION
Name of Assignee)	(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)
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